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10/587,607	07/27/2006	Francesco Pessolano	NL040077US1	9957

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EXAMINER	
BAE, JI H	

ART UNIT	PAPER NUMBER
2115	

NOTIFICATION DATE	DELIVERY MODE
12/18/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/587,607	PESSOLANO, FRANCESCO	
	Examiner	Art Unit	
	JI H. BAE	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed on 19 September 2008 have been fully considered but they are not persuasive. Applicant's amendments have introduced new matter and/or are unsupported by the originally filed specification and claims.

The examiner finds that applicant's invention ***as disclosed in the originally filed specification*** comprises two main aspects:

1. A method/apparatus for determining a maximum clock frequency for a processing system, wherein a clock frequency is set to an initial frequency and then repeatedly increased until a maximum frequency is identified at which timing constraints are not violated (e.g. Fig. 2).
2. A method/apparatus for determining that a processing system requires a temporary increase in performance, raising a clock frequency of the processing system to the maximum frequency previously determined, and then lowering the clock frequency to the original nominal value (e.g. pp. 9, lines 1-5).

With respect to the second aspect of applicant's invention, applicant has disclosed two distinct embodiments:

A. Raising the clock frequency for a processing system by programming a programmable ring oscillator to produce a clock signal with a higher frequency (i.e. Fig. 1).

B. Raising the clock frequency for a processing system by using a clock multiplexer to switch from an externally provided nominal frequency to an internally generated maximum clock frequency (i.e. Fig. 3).

Applicant's amendments introduce new matter and/or are unsupported by the original specification because they do not claim the invention as it has been disclosed. Instead, applicant's amendments conflate the various embodiments/aspects of the invention in such a way that is not envisioned by the disclosure.

Regarding claims 1 and 4-7, applicant has amended the claims to recite that the timing monitor ***"monitors a level of input and output buffers to prevent said output buffers from being starved of data while said input buffers include data that is blocked from said processing system".*** Applicant cited pp. 9, lines 6-15 of the specification as allegedly providing support for the amendment. The examiner respectfully disagrees with the applicant's assertion that this section of the specification, or any other, provides support for this amendment.

The portion of the disclosure cited by the applicant teaches that it may be necessary to raise the clock frequency of a system when, for example, an ***"output is starving (i.e. no output data is ready yet) while the inputs are blocked (i.e. new input data is waiting for the current data to be processed)".*** Additionally, such situations can be detected ***"by knowing either the state of the system of the state of the I/O queues (when present)".***

There is no teaching in the cited portion of the specification, or any other portion, that the ***timing monitor monitors input and output buffers.*** While this section of the specification discusses the general scenario outlined in applicant's amendment, it does not teach that input and output buffers are in view, and does not even use the term

"buffers". But even if input and output buffers were in view, there is no evidence that the specification assigns the responsibility of monitoring input and output buffers to the timing monitor. The context of pp. 9, lines 6-15 is directed towards method (2) as outlined above -- i.e., the situation described is one scenario in which the clock frequency of the processing system would be temporarily increased to the maximum clock frequency. But claim 1 is directed towards method (1) as outlined above. In other words, even if one were to grant that pp. 9, lines 6-15 taught the monitoring of input/output buffers (which the examiner maintains it does not), it does not teach it in the context of determining a maximum clock frequency. Rather, this portion of the specification is concerned with method (2) -- raising the nominal frequency to the maximum ***after the maximum frequency has already been determined***. This comports with previous sections of the disclosure that teach ***the function of the timing monitor is to ensure timing constraints are met during method (1)***, and not to determine when the nominal frequency is to be raised according to method (2).

Regarding claim 12, applicant has amended the claim to recite that the clock generation means comprises a first and second clock generation means, wherein the switch means switches from the second clock generation means to the first clock generation means when a request to increase the clock frequency is received. The examiner submits that this amendment is also unsupported by the original specification.

Claim 12 is dependent from claim 7. Claim 7 is directed towards embodiment A as outlined above. This is evidenced by the fact that the clam recites a "programmable clock generation means" that generates ***both the nominal and the maximum clock frequency***. On the other hand, claim 12 is directed towards embodiment B. This is evidenced by the fact claim 12 recites two clock generation means with a switch means to switch between them.

Applicant has not taught that embodiments A and B are useable together. It is clear that these are two separate embodiments. The maximum clock frequency may be provided be either (1) reprogramming the programming ring oscillator of embodiment A to a new frequency, or (2) switching the clock mux to select the internal clock rather than the external clock as in embodiment B.

Additionally, applicant's amendment to claim 12 recites that the clock generation means comprises the first and second clock generation means. The only previous recitation of a clock generation means is in claim 7, which recites a "programmable clock generation means". This is clearly a reference to the programmable ring oscillator of either Fig. 1 or 3. According to the amendments then, the ring oscillator is comprised of a first and second clock generation means which are switched between to provide the nominal and maximum clock frequencies. But this is clearly not taught in the specification. Fig. 3 teaches two separate clock generation means, one of which is a programmable ring oscillator, and neither of which is comprised of the other. Pp. 9, lines 15-34 repeatedly teach that one clock generation means is "external" while the other is "internal". Based on this, the examiner further submits that neither clock generation means can be said comprise the other, since they are explicitly taught as being separate.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter

which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Applicant's amendments to claims 1, 4-7, and 12 comprise new matter and/or are unsupported by the originally filed specification. See "Response to Arguments" above.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4 and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Klock et al., U.S. Patent No. 7,382,366.

Regarding claim 1, Klock teaches a method comprising:

generating a clock signal at an initial frequency **[col. 5, line 10-12, clock has a default setting]**;

increasing the initial frequency in a step-wise manner **[col. 4, lines 43-47, increasing the clock frequency by 0.5 MHz or 1 MHz increments]**, and determining the operation of the system at each of a selected number of frequencies until a clock frequency is identified at which the processor does not operate correctly **[col. 4, lines 39-47, stress testing and detecting failures]**; and

identifying a maximum clock frequency at which the system can operate correctly, characterized in that:

the maximum clock frequency comprises the frequency immediately previous to the one identified as being one at which the system does not operate correctly **[col. 4, lines 47-49, highest overclocking parameters that pass the stress test]**; and in that

a timing monitor is provided for determining whether or not the system can operate within system timing constraints at each frequency, thereby indicating whether or not the system operates correctly at the respective frequency **[col. 3, lines 39-51, overclocking control module includes performance monitoring functionality, graphics pipeline stress tester detects errors generated by a test sequence]**.

Regarding claim 2, Klock teaches storing the maximum frequency in memory **[col. 5, lines 23-38, internal table stores maximum clock rates]**.

Regarding claim 3, Klock teaches periodically performing the method of claim 1 while the system is running **[Fig. 5]**. Fig. 5 shows that after the stress test fails, the system selects a clock frequency below the failing frequency with sufficient margin **[Fig. 5, step 570]**, and returns to the beginning step 520, wherein the method may be repeated.

Regarding claim 4, Klock teaches the method of claim 1, and also the apparatus with means to execute the claimed method.

Regarding claim 9, Klock teaches a frequency finder for increasing the frequency of the clock signal from the initial frequency to the maximum frequency **[Fig. 2, clock controller]**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to

> be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Klock in view of applicant's admission of prior art. Although Klock does not explicitly teach that the clock generators in Fig. 2 are ring oscillators, applicant teaches that ring oscillators are known in the art, and cites an exemplary patent reference **[pp. 8, lines 17-20]**. Since ring oscillators are known in the art as clock generators, it would have been obvious to one of ordinary skill in the art to include applicant's admitted prior art in the system of Klock as an obvious variation of the clock generators taught by Klock in Fig. 2.

Claims 5, 7, 8, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams, U.S. Patent No. 5,774,704, in view of Rosno et al., U.S. Patent No. 6,535,986. Both Williams and Rosno are applicant-cited references.

Regarding claim 5, Williams teaches a method comprising:

generating, after reset, a clock signal at a nominal frequency, less than the maximum frequency **[Fig. 5A, step 502, initial clock frequency]**, until a signal is received indicating that an increased clock frequency is required **[Fig. 5A, steps 505 and 506, max clock frequency required due to high processor load]**;

generating, in response to receipt of the signal, a clock signal at the maximum frequency for a required time **[Fig. 5A, step 506, clock frequency increased to maximum]**; and then

once again generating a clock frequency at the nominal frequency **[col. 7, lines 1-4, process repeats, going back to Fig. 5A, step 503, if high load not detected and clock frequency is maximum from a previous setting, then clock frequency is decreased, step 507 and 508]**.

Although the method taught by Williams teaches setting a predetermined maximum clock frequency, Williams does not teach determining a maximum clock frequency at which the system can operate within system timing constraints.

Rosno teaches a method comprising:

determining, when the system is reset **[col. 6, lines 15-16, method is performed at every initial program load]**, a maximum clock frequency at which the system can operate within system timing constraints **[col. 6, lines 1-11, highest possible frequency with acceptable timing margin]**.

It would have been obvious to one of ordinary skill in the art to combine the teachings of Williams and Rosno by implementing the method of Rosno in the system of Williams to determine the maximum clock frequency taught by Williams. The system of Williams assumes the existence of some predetermined maximum clock frequency, but does not disclose a method for determining the maximum clock frequency. Rosno's background disclosure teaches that it is not desirable to simply run a clock at the fastest possible frequency, since violations of timing margins can lead to erroneous operations **[col. 2, lines 1-12]**. Therefore, it would have been obvious to one of ordinary skill in the art to implement the method of Rosno in the system of Williams, with the predictable result that Rosno would have provided a method to determine a maximum clock frequency for Williams. Additionally, the method of Rosno would have improved Williams by providing a clock frequency with sufficient timing margin to prevent errors during operation.

Regarding claim 7, Rosno teaches the method of claim 5, and also the apparatus with means to execute the claimed method.

Regarding claim 8, Rosno teaches a timing monitor for monitoring system timing constraints **[Fig. 1, state machine or service processor, col. 5, lines 53-60, state machine or service processor detects errors at the given clock frequency setting]**.

Regarding claim 11, Rosno teaches a frequency finder and selector for determining the maximum frequency at reset **[col. 5, lines 18-42, state machine, frequency synthesizer, PLL/DM/SCC control clock frequency and settings]**. Williams teaches receiving a request for an increase in clock frequency and causing the clock generation means to generate a clock signal at the maximum frequency until the request expires or is withdrawn **[Fig. 5A, steps 505 and 506, max clock frequency required due to high processor load, col. 7, lines 1-4, process repeats, going back to Fig. 5A, step 503, if high load not detected and clock frequency is maximum from a previous setting, then clock frequency is decreased, step 507 and 508]**.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the

advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JI H. BAE whose telephone number is (571)272-7181. The examiner can normally be reached on Monday-Friday, 10 am to 6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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